

***ME* DISPLAYS**

SPECIFICATIONS

FOR

LCD MODULE

SG240128D

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• **FEATURES**

Number of Dots	240 x 128
Duty Cycle	1/128 Duty
Power Supply	5V
Backlight Options	Edge Lighting Type CCFL Edge Lighting Type LED
Recommended Controller	HD64646, MSM6225, SED1335

• **MECHANICAL PARAMETERS**

Module Size	144.0W x 104.0H x 10.3T mm
Viewing Area Size	114.0W x 64.0H mm
Active Area Size	107.95W x 57.55H mm
Dot Size	0.40 x 0.40 mm
Dot Pitch	0.45 x 0.45 mm

• **ABSOLUTE MAXIMUM**

Item	Symbol	Min.	Max	Unit
Supply Voltage for Logic	$V_{DD} - V_{SS}$	0	+7.0	V
Supply Voltage for LCD Drive	$V_{DD} - V_O$	0	+28.0	V
Input Voltage	V_i	V_{SS}	V_{DD}	V
Operating Temperature	T_a	0	+50	C
Storage Temperature	T_{stg}	-10	+60	C

• **ELECTRICAL CHARACTERISTICS**

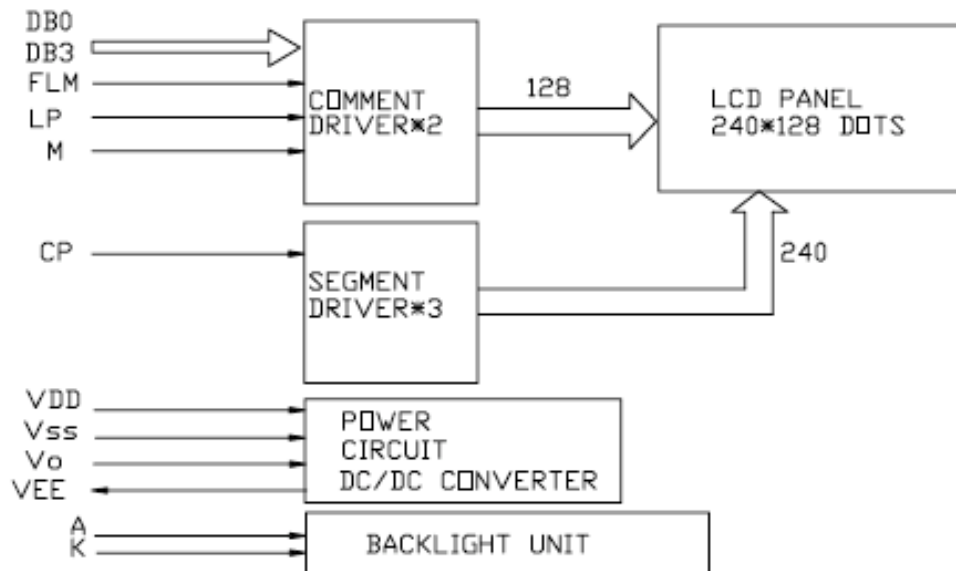
Item	Symbol	Condition	Min	Typ	Max	U
Power Supply Voltage for Logic	$V_{DD} - V_{SS}$	--	4.5	5.0	5.5	V
Power Supply Voltage for LCD	$V_{DD} - V_O$	$V_{DD}=5V$ $T_a=25C$	16.9	18.0	19.2	V
Input "High" Voltage(1)	V_{ih}	--	2.2	--	V_{DD}	V
Input "Low" Voltage(1)	V_{il}	--	--	--	0.6	V
Output "High" Voltage(1)	V_{oh}	--	2.4	--	--	V
Output "Low" Voltage(1)	V_{ol}	--	--	--	0.4	V
Power Supply Current	I_{DD}	$V_{DD} = 5.0V$	--	15	24	mA

(1) Applied to terminals CS1, CS2, DB0~DB7, R/W, D/I, E RST

• PIN ASSIGNMENT

No.	Symbol	Level	Function
1	FLM	H	Frame Start Signal
2	M	H/L	Control Signal for AC Driving
3	LP	H→L	Common Driver Data Shift Signal
4	CP	H→L	Clock Pulse For Segment Shift Register
5	V _{DD}	5V	Power Supply Voltage
6	V _{SS}	0V	Power Supply Ground
7	V _{EE}	--	Power Supply Voltage for LCD
8	DB0	H/L	Data Bit0
9	DB1	H/L	Data Bit1
10	DB2	H/L	Data Bit2
11	DB3	H/L	Data Bit3
12	V _O	--	Contrast Adjustment Voltage
13	NC	--	No Connection

• BLOCK DIAGRAM



• **TIMING CHARACTERISTICS**

Item	Symbol	Min	Max	Unit
Frequency of Maximum Clock	f_{CP}	--	8	MHZ
CL1, CL2, Pulse Width	t_W	45	--	ns
Rise, Fall Time	t_R, t_F	--	15	ns
Data Setup Time	t_{DSU}	20	--	ns
Data Hold Time	t_{DHD}	20	--	ns
CL1 Setup Time	t_{LSU}	80	--	ns
CL1 → CL2 Time	t_{LC}	80	--	ns
FLM Setup Time	t_{SETUP}	100	--	ns
FLM Hold Time	T_{HOLD}	100	--	ns
M Delay Time	t_{DF}	--	300	ns

• **TIMING DIAGRAMS**

